

[METHOD OF FABRICATING A VERTICAL MOS TRANSISTOR]

Abstract of Disclosure

A gate mask is formed on a silicon substrate of a semiconductor wafer followed by etching region of the silicon substrate not covered by the gate mask to a predetermined depth. Subsequently, a silicon oxide layer is formed on the region of the silicon substrate not covered by the gate mask. A first conductive layer and a second conductive layer are formed respectively on the silicon substrate. Then, a first etching back process is performed to form a spacer consisting of the second conductive layer, the first conductive layer and the silicon oxide layer on the region of the silicon substrate below the gate mask. After the gate mask is removed, a selective etching process is performed to remove portions of both the first conductive layer and the silicon oxide layer to form the spacer into an undercut profile. Finally, a doping process and an ion implantation process are performed, respectively, to form lightly doped drains (LDDs) and a source/drain (S/D) of a vertical MOS transistor.

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